REMARKS

The applicants appreciate the examiner's thorough examination of the subject application and request reexamination and reconsideration of the subject application in view of the preceding amendments and the following remarks.

Concerning item 1 of the subject action, the examiner objects to claims 4, 21 and 35 for various technical reasons. The applicants have amended claims 4, 21 and 35 to address the issues raised by the examiner.

Concerning items 2-21 of the subject action, the examiner rejects claims 1, 5-6, 9-14, 18, 22-23, and 26-31, under 35 USC §102(e), based on the teachings of Tanaka et al (U.S. Publication No.: US2001/0018758).

With respect to claim 1, applicants have amended claim 1 to include the subject matter of claim 2, namely "providing the circuit designer with feedback concerning the physical characteristic of the circuit being designed". As claim 2 (which has been canceled) was not rejected based on the teachings of Tanaka, applicants respectfully assert that amended claim 1 (which includes the subject matter of cancelled claim 2) is allowable with respect to Tanaka et al.

With respect to claims 5-6 and 9-14, each of these claims depends (either directly or indirectly) on amended claim 1 (an allowable base claim). Accordingly, applicants respectfully asserts that claims 5-6 and 9-14 are allowable with respect to Tanaka et al.

With respect to claim 18, applicants have amended claim 18 to include the subject matter of claim 19, namely "a feedback display process for providing the circuit designer with feedback concerning said physical characteristic of said circuit being designed". As claim 19 (which has been canceled) was not rejected based on the teachings of Tanaka, applicants respectfully assert that amended claim 18 (which includes the subject matter of cancelled claim 19) is allowable with respect to Tanaka et al.

With respect to claims 22-23 and 26-31, each of these claims depends (either directly or indirectly) on amended claim 18 (an allowable base claim). Accordingly, applicants respectfully assert that claims 22-23 and 26-31 are allowable with respect to Tanaka et al.

Concerning items 22-45 of the subject action, the examiner rejects claims 1-4, 7-8, 15-21, 24-25, and 32-38, under 35 USC §102(b), based on the teachings of Watkins (U.S. Patent No.: 5,666,289).

With respect to claim 1, applicants claim (in amended claim 1):

> a method of designing a semiconductor device, the method comprising: (a) maintaining a circuit design parameter file for a circuit being designed, the circuit design parameter file specifying a physical characteristic of the circuit; (b) monitoring a design environment to detect the addition of a circuitry component to the circuit; (c) accessing a component design parameter file that specifies at least one design parameter for that added circuitry component; (d) updating the circuit design parameter file based on the at least one design parameter included in the component design parameter file; and (e) providing the circuit designer with feedback concerning the physical characteristic of the circuit being designed.

Watkins fails to disclose elements any of the elements (namely elements a-b) of the applicants claimed invention and, therefore, is not a proper basis for a 35 USC §102(b) rejection. Accordingly, applicants respectfully assert that claim 1 is allowable.

Specifically, the applicants claimed invention concerning a circuitry design system in which a circuit design parameter file is maintained for a circuit being designed. The design environment is monitored to detect when components are added to this circuit. In the event of such an addition, a component design parameter file, which relates to the component being added, is accessed and the circuit design parameter file is updated to include information relating to the recently added component. The circuit designer can also be provided with feedback concerning the physical characteristics of the circuit being designed.

As stated above, the circuit design parameter file is maintained during the design of the circuit and as components are added to the circuit, the circuit design parameter file is updated to reflect these additions. Watkins fails to disclose the use of such a file. The examiner relies of Watkins, col. 6, line 54 to col. 7, line 3 to disclosure the use of such a file. The applicants direct the examiner's attention to Watkins, col. 5, line 66 to col. 6, line 2. Specifically, this passages states that "once the desired designed has been achieved, a network list file (".NETLIST") of the design may be created. A design symbol and network may also be saved in a file called "<design>.def." (*emphasis added*). Note that the file that describes the circuit (i.e., the

.NETLIST file) is not created until after the circuit is designed. This position is further reinforced by reviewing Watkins, col. 6, line 8 through col. 7, line 50. It is clear from this passage that Watkins discloses a system in which a circuit is designed, a file is created defining that circuit, and then numerous error checking / calculation processes are employed to determine the circuit's characteristics. From this passage it is clear that the ".LIB" and ".TECHLIB" files relied upon by the examiner do not perform the function of the applicants' circuit design parameter file, as the design process disclosed in Watkins in not an iterative design process, as claimed by the applicants. The Watkins process requires the circuit to be designed prior to the creation of the file defining the circuit. Once this file is created, the file can be processed by a string of stand alone processes.

Conversely, the applicants' claimed invention maintains the circuit design parameter file during the circuit design process and this file is updated and modified as the circuit design evolves. This is quite distinguishable from the Watkins system, in which the circuit is completely designed prior to the creation of the file defining the circuit.

Concerning element (b) of the applicants' claimed invention, the examiner relies of Watkins, col. 8, lines 29-37, to disclose this element. However, this passage states that "any minor logic changes made after running the LPACE 64, can be in [sic] evaluated through an interim design by running an abbreviated simulation sequence involving the LCMP 51, LLINK 52, LDEL 61, and LSIM 95 programs. The final design must, however, be evaluated more thoroughly by rerunning the LVER 54 program (to update the .DESIGN 55 and .PADREF 56 files) and the Bonding Diagram program 57 prior to obtaining sign-off on the final design".

From this passage in Watkins, it is clear that this feature of Watkins in not functionally equivalent to "monitoring a design environment to detect the addition of a circuitry component to the circuit" (element (b) of applicants' amended claim 1). The applicants claimed invention monitors a design environment to determine the addition of circuitry component(s) to the circuit being designed. As discussed above, when using the Watkins device, the circuit is designed first, then a file is created to design the circuit, then that file is processed to analyze the circuit. In the event that "minor changes" are required, an "abbreviated simulation sequence" can be run. However, the "final design" must be reevaluated more thoroughly by rerunning the previously

run evaluation programs. Note that the "abbreviated design sequence" comprises running the LCMP, LLINK, LDEL, and LSIM, and therefore this "abbreviated design sequence" is simply a portion of the previously run evaluation programs. Therefore, this passage does not describe a system that monitors the design environment, as the circuit is already designed and the "abbreviated simulation sequence" merely constitutes rerunning a portion of the previously run evaluation programs. This is quite distinguishable from the applicants' claimed invention, in which the design environment is monitored to determine the addition of a circuitry component to the circuit.

Concerning elements (c) and (d) of the applicants' amended claim 1, the examiner relies of Watkins, col. 8, lines 37-47, to disclose these elements. This passage does not disclose "accessing a component design parameter file that specifies at least one design parameter for that added circuitry component, and updating the circuit design parameter file based on the at least one design parameter included in the component design parameter file". As discussed above, the files that are described in this passage are generated by the LPACE program, which is the last of a string of evaluation programs described above. Again, the applicants wish to remind the examiner that these programs are run once the design process is completed and, therefore, do not disclose the applicants' claimed invention which includes "accessing a component design parameter file that specifies at least one design parameter for that added circuitry component, and updating the circuit design parameter file based on the at least one design parameter included in the component design parameter file".

Concerning element (e) of the applicants' amended claim 1, the examiner relies of Watkins, col. 5, lines 54-63, to disclose these elements. The applicants respectfully assert that this passage cannot disclose element (e) of the applicants' claimed invention, due to the functionality of the application. Specifically and as discussed above, when using the Watkins system, the circuit is first designed and specified in the form of a file. Once this file is completed, that file is processed and the circuit is analyzed. Accordingly, Watkins, col. 5, lines 54-63, merely discusses the generation of the file defining the circuit and not the analysis of the circuit. And since the analysis does not begin until after the file (and, therefore, the circuit) is

completely defined, this passage cannot disclose "providing the circuit designer with feedback concerning the physical characteristic of the circuit being designed".

Accordingly, applicants respectfully assert that amended claim 1 (which includes the subject matter of cancelled claim 2) is allowable with respect to Watkins.

With respect to claim 2, applicants have cancelled this claim.

With respect to claims 3-4, 7-8, and 15-17, each of these claims depends (either directly or indirectly) on amended claim 1 (an allowable base claim). Accordingly, applicants respectfully assert that claims 3-4, 7-8, and 15-17 are allowable with respect to Watkins.

With respect to amended claim 18, this claim is rejected based on the same passages relied upon by the examiner to reject claim 1. Applicants respectfully reiterate the arguments discussed above concerning claim 1. Accordingly, applicants respectfully assert that amended claim 18 (which includes the subject matter of cancelled claim 19) is allowable with respect to Watkins.

With respect to claim 19, applicants have cancelled this claim.

With respect to claims 20-21, 24-25, and 32-34, each of these claims depends (either directly or indirectly) on amended claim 18 (an allowable base claim). Accordingly, applicants respectfully assert that claims 20-21, 24-25, and 32-34 are allowable with respect to Watkins.

With respect to amended claim 35, this claim is rejected based on the same passages relied upon by the examiner to reject claim 1. Applicants respectfully reiterate the arguments discussed above concerning claim 1. Accordingly, applicants respectfully assert that amended claim 35 (which includes the element of "provide the circuit designer with feedback concerning the physical characteristic of the circuit being designed") is allowable with respect to Watkins.

With respect to claim 36, this claim directly depends on amended claim 35 (an allowable base claim). Accordingly, applicants respectfully assert that claim 36 is allowable with respect to Watkins.

With respect to claim 37, this claim is rejected based on the same passages relied upon by the examiner to reject claim 1. Applicants respectfully reiterate the arguments discussed above concerning claim 1. Accordingly, applicants respectfully assert that amended claim 37 (which

includes the element of "provide the circuit designer with feedback concerning the physical characteristic of the circuit being designed") is allowable with respect to Watkins.

With respect to claim 38, this claim directly depends on amended claim 37 (an allowable base claim). Accordingly, applicants respectfully assert that claim 38 is allowable with respect to Watkins.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Enclosed is a $110 check for the Petition for Extension of Time fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: October 21, 2002

Brian J. Colandreo
Reg. No. 42,427

Fish & Richardson P.C.
225 Franklin Street
Boston, Massachusetts 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

Version with markings to show changes made

In the claims:

Claims 2 and 19 have been cancelled.

Claims 1, 4, 18, 21, 35 and 37 has been amended as follows:

1. A method of designing a semiconductor device, the method comprising:

maintaining a circuit design parameter file for a circuit being designed, the circuit design parameter file specifying a physical characteristic of the circuit;

monitoring a design environment to detect the addition of a circuitry component to the circuit;

accessing a component design parameter file that specifies at least one design parameter for that added circuitry component; [and]

updating the circuit design parameter file based on the at least one design parameter included in the component design parameter file; and

providing the circuit designer with feedback concerning the physical characteristic of the circuit being designed.

4. The method of claim 3 further comprising providing the circuit designer with feedback concerning the physical characteristic of the circuit being designed in response to the circuit designer requesting [the same] feedback.

18. An estimation process for designing a semiconductor device comprising:

a parameter file maintenance process for maintaining a circuit design parameter file for a circuit being designed, the circuit design parameter file specifying a physical characteristic of said circuit;

a design space monitoring process for monitoring a design environment to detect the addition of a circuitry component to said circuit;

a component file access process for accessing a component design parameter file that specifies at least one design parameter for said added circuitry component; [and]

a parameter file updating process for updating said circuit design parameter file based on said at least one design parameter included in said component design parameter file; and

a feedback display process for providing the circuit designer with feedback concerning said physical characteristic of said circuit being designed.

21. The process of claim 20 further comprising a feedback display process for providing the circuit designer with feedback concerning said physical characteristic of said circuit being designed in response to the circuit designer requesting [the same] feedback.

35. A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by [the] a processor, cause that processor to:

maintain a circuit design parameter file for a circuit being designed by a circuit designer, wherein the circuit design parameter file specifies a physical characteristic of the circuit;

monitor a design environment to detect the addition of a circuitry component to the circuit;

access a component design parameter file that specifies at least one design parameter for that added circuitry component; [and]

update the circuit design parameter file based on the at least one design parameter included in the component design parameter file; and

provide the circuit designer with feedback concerning the physical characteristic of the circuit being designed.

37. A processor and memory configured to:

maintain a circuit design parameter file for a circuit being designed by a circuit designer, wherein the circuit design parameter file specifies a physical characteristic of the circuit;

monitor a design environment to detect the addition of a circuitry component to the circuit;

access a component design parameter file that specifies at least one design parameter for that added circuitry component; [and]

update the circuit design parameter file based on the at least one design parameter included in the component design parameter file; and

provide the circuit designer with feedback concerning the physical characteristic of the circuit being designed.

In the abstract:

A [method comprising maintaining a] circuit design parameter file is maintained for a circuit being designed by a circuit designer. [The] This circuit design parameter file specifies a physical characteristic of the circuit. [The method monitors a] A design environment is monitored to detect the addition of a circuitry component to the circuit and [accesses] a component design parameter file that specifies at least one design parameter for that added circuitry component is accessed. The [method updates the] circuit design parameter file is updated based on the [at least one] design parameter(s) included in the component design parameter file. The circuit designer is provided with feedback concerning the physical characteristic of the circuit being designed.